

Specifications for Approval

TFT MODULE

MODEL:ET055RFPB93

Ver:A

CUSTOMER'S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWD	PD REVIEWD	PREPARED By
KEN		BOSE	J.N

◆ This specification is subject to change without notice. Please contact or its representative before designing your product based on this specification.

Records of Revision

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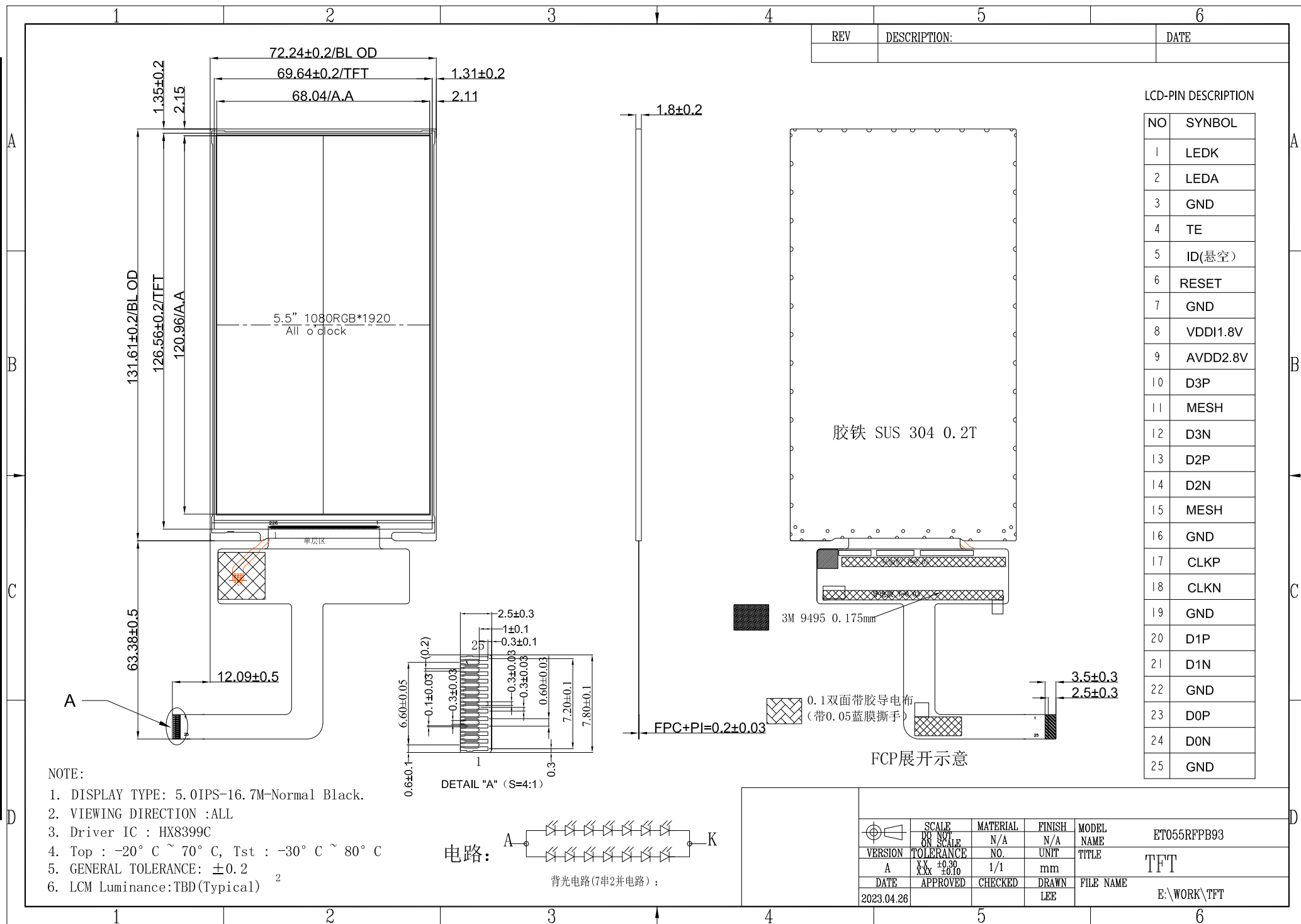
Contents

1. General Specification.....	4
2. Mechanical Drawing.....	5
3. Block Diagram.....	6
4. Interface Pin Function.....	7
5. Absolute Maximum Ratings.....	9
6. Electrical Characteristics.....	9
7. Optical Characteristics.....	10
8. Operating Instructions.....	13
9. Standard Specification for Reliability.....	19
10. Specification of Quality Assutance.....	21
11. General Precautions.....	29
12. Packing Method.....	29

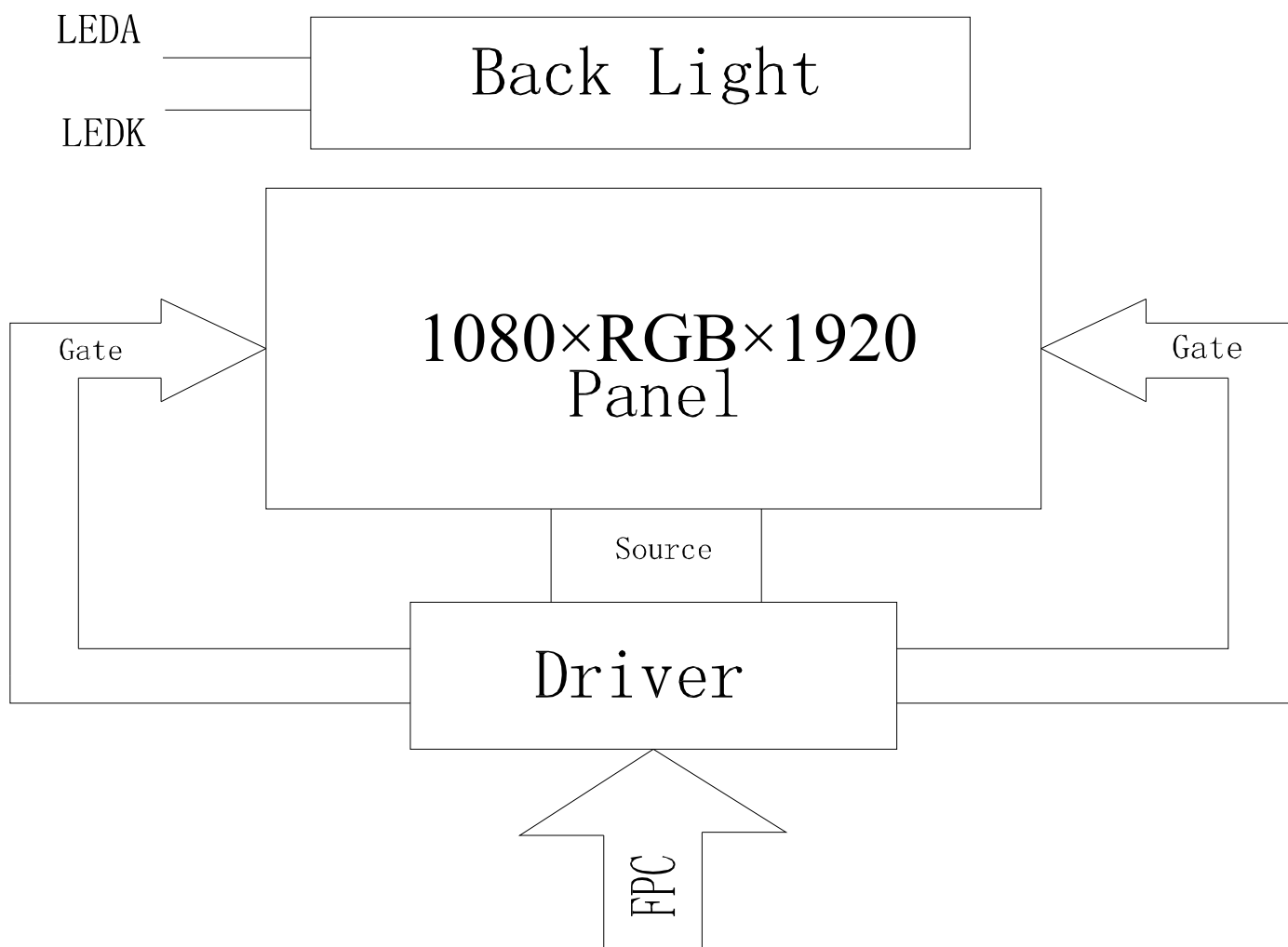
1. General Specification

Item	Specification	Unit
LCD Size	5.5	Inch
Panel Type	A-SI TFT	
Resolution	1080xRGBx1920	Pixel
Display Mode	Normally Black	-
Number of Colors	16.7M	-
Viewing Direction	ALL	-
NTSC	68%	-
Contrast Ratio	800	-
Luminance	350	cd/m2
Module Size	72.24x131.61x1.8	mm
Panel Active Area	68.04(H)x120.96(V)	mm
Pixel Pitch	0.063×0.063	mm
Pixel Arrangement	RGB Vertical Stripe	
Weight	TBD	-
Driver IC	HX8399C	
WITH TP	Without TP	
Light Source	7S2P	-
Interface	Mipi	-

Product Specification



3. Block Diagram



4. Interface Pin Function

No.	Symbol	Function
1	LEDK	Backlight cathode.
2	LEDA	Backlight anode.
3	GND	Ground
4	TE	Tearing effect output
5	ID	LCD ID
6	RESET	Reset pin
7	GND	Ground
8	VDDI1.8V	power supply 1.8V
9	AVDD2.8V	power supply 2.8V
10	D3P	MIPI DSI 3 lane(+)
11	MESH	mesh
12	D3N	MIPI DSI 3 lane(-)
13	D2P	MIPI DSI 2 lane(+)
14	D2N	MIPI DSI 2 lane(+)
15	MESH	mesh
16	GND	Ground
17	CLKP	MIPI DSI CLK(+)
18	CLKN	MIPI DSI CLK(-)
19	GND	Ground
20	D1P	MIPI DSI 1 lane(+)
21	D1N	MIPI DSI 1 lane(-)
22	GND	Ground
23	D0P	MIPI DSI 0 lane(+)
24	D0N	MIPI DSI 0 lane(-)
25	GND	Ground

5. Absolute Maximum Ratings

Item	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	AVDD	-0.3	6.0	V	
Logic Supply Voltage	VDDI	-0.3	3.6	V	
Operating Temperature	Top	-20	70	°C	
Storage Temperature	Tst	-□0	80	°C	
Relative Humidity Note2	RH	--	≤95	%	Ta≤40°C
		--	≤85	%	40°C<Ta≤50°C
		--	≤55	%	0°C<Ta≤60°C
		--	≤36	%	60°C<Ta≤70°C
		--	≤24	%	70°C<Ta≤80°C
Absolute Humidity	AH	--	≤70	g/m3	Ta>70°C

6. Electrical Characteristics

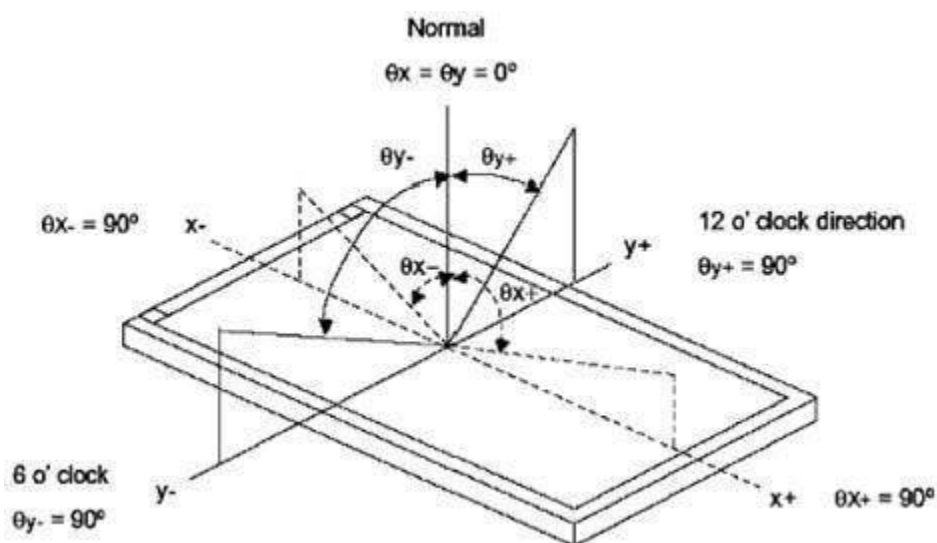
Item		Symbol	MIN	TYP	MAX	Unit
Analog operating voltage		AVDD	2.7	2.8	2.9	V
Logic operating voltage		VDDI	1.65	1.8	3.6	V
Input Signal Voltage	High Level	VIH	0.7*VDDI	-	VDDI	V
	Low Level	VIL	-0.3	-	0.3*VDDI	
Output Voltage	High Level	VOH	0.8DDI	-	VDDI	
	Low Level	VOL	0	-	0.2VDDI	

6.2 Current for LED Driver

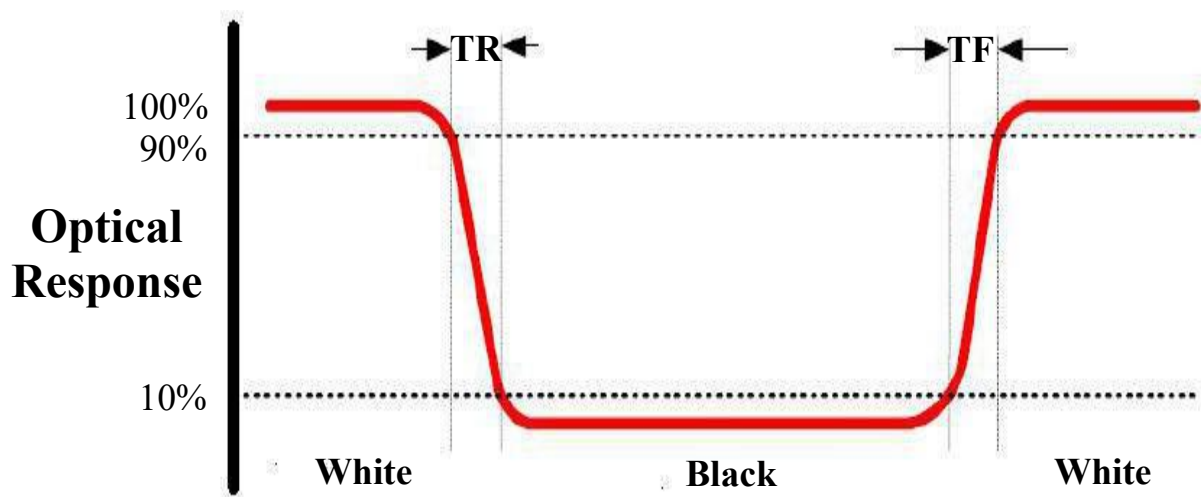
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	--	40	50	mA	14 LEDs (7 LED Serial, 2 LED Parallel)
Forward Current Voltage	VF	21.0	22.4	23.8	V	
Power Consumption	WBL	--	896	--	mW	
LED life time	--	10000	(20000)	--	Hrs	

7. Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit
View Angles		θT	CR≥10	75	80		Degree
		θB		75	80		
		θI		75	80		
		θR		75	80		
Contrast Ratio		CR	θ=0°	600	800		
Response Time		TON	25°C	-	25	35	ms
		TOFF					
Chromaticity	White	X	Backlight is on	0.237	0.277	0.317	
		y		0.259	0.299	0.339	
	Red	X					
		y					
	Green	X					
		y					
	Blue	X					
		y					
Uniformity		U	-	80	85	-	%
NTSC		-	-	60	68	-	%
Luminance		L	-	300	350	-	Cd/m2

Note 1: Definition of Viewing Angle θ_x and θ_y :**Note 2: Definition of contrast ratio CR:**

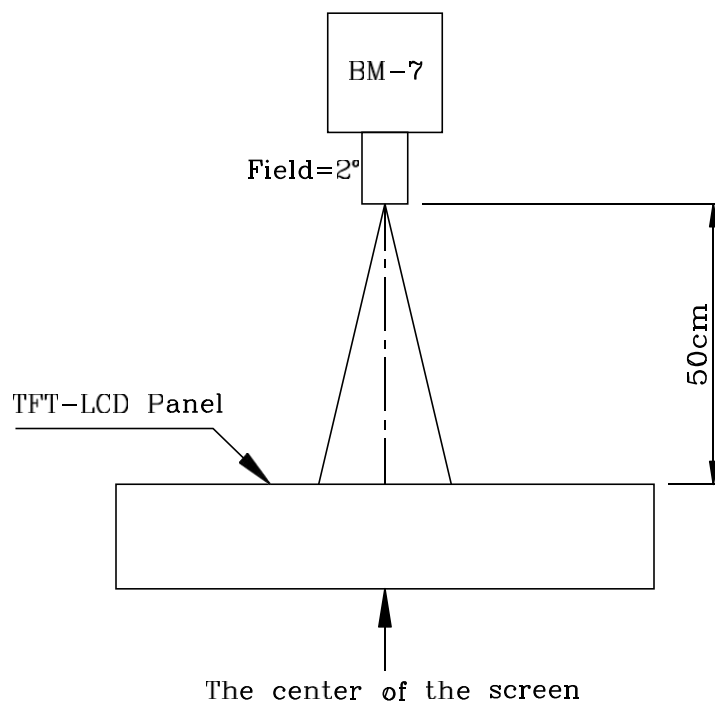
$$CR = \frac{\text{Lum i nance of w h i t e s t a t e}}{\text{Lum i nance of b l a c k s t a t e}}$$

Note 3: Definition of Response Time(T_r , T_f)

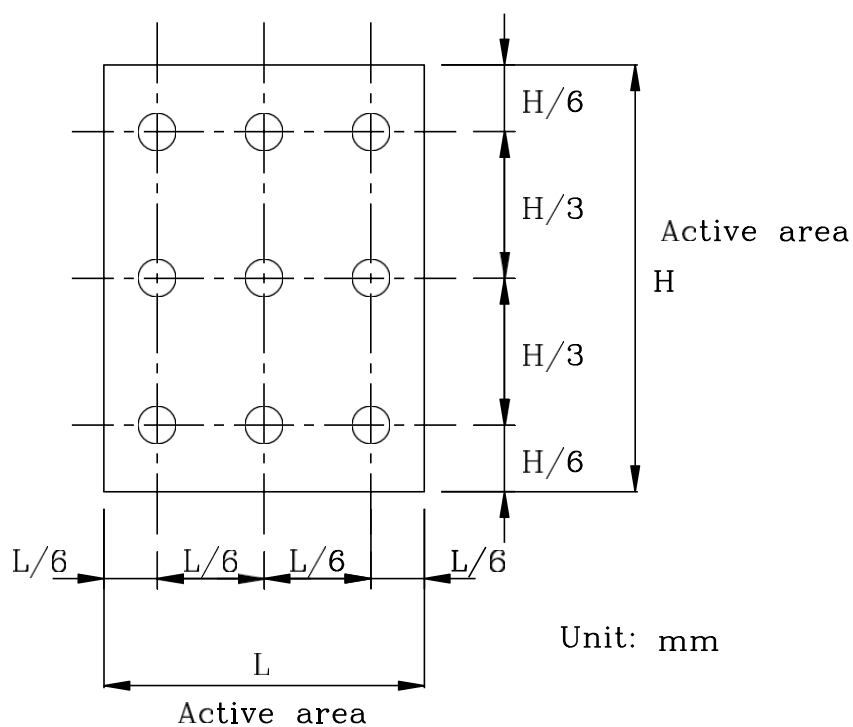
Note 4: Definition of Luminance

①The Brightness Test Equipment Setup

Field= 2° (As measuring “black” image, field= 2° is the best testing condition)



②The Brightness Test Point Setup



8. Operating Instructions

DC characteristics

(VSP=4.8 to 6V, VSN=-4.8 to -6, VDD1=1.65 to 3.3V, T_A=-40 to 85 °C)

Parameter	Symbol	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
Input high voltage	V _{IH}	VDD1= 1.65 ~ 3.3V	0.7 VDD1	-	VDD1	V
Input low voltage	V _{IL}		0	-	0.3 VDD1	V
VPP	V _{IH} V _{IL}	VPP	7.25V	7.5V	7.75V	V
Output high voltage (SDO, CABC_PWM_OUT)	V _{OH1}	I _{OH} = -1.0 mA	0.8 VDD1	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT)	V _{OL1}	VDD1= 1.65 ~ 2.4V I _{OL} = 1.0 mA	0	-	0.2 VDD1	V
Logic High level input current	I _{IH}	VSYNC, HSYNC	-	-	1	μA
		RESX, DCX, CSX, SCL	-	-	1	μA
	I _{IHD}	DB[7...0], SDI_SDA, DCX	-	-	1	μA
		DB[7...0]	-	-	1	μA
Logic Low level input current	I _{IL}	VSYNC, HSYNC	-1	-	-	μA
		RESX, DCX, CSX, SCL	-1	-	-	μA
	I _{ILD}	DB[7...0], SDI_SDA, DCX	-1	-	-	μA
		DB[7...0]	-1	-	-	μA
Current consumption Sleep in mode (VSP-VSSA)	I _{ST(VSP)}	VDD3=2.8V, VDD1=1.8V, HS_VCC T _A =25°C	-	-	TBD	μA
Current consumption Sleep in mode (VSN-VSSA)	I _{ST(VSN)}		-	-	TBD	μA
Current consumption Sleep in mode (VDD1-VSSD)	I _{ST(VDD1)}		-	-	TBD	μA
Current consumption Sleep in mode (HS_VCC-HS_VSS)	I _{ST(HS_VCC)}		-	-	TBD	μA
Current consumption Deep Sleep in mode (VSP-VSSA)	I _{DST(VSP)}		-	-	TBD	μA
Current consumption Deep Sleep in mode (VSN-VSSA)	I _{DST(VSN)}		-	-	TBD	μA
Current consumption Deep Sleep in mode (VDD1-VSSD)	I _{DST(VDD1)}		-	-	TBD	μA
Current consumption Deep Sleep in mode (HS_VCC-HS_VSS)	I _{DST(HS_VCC)}		-	-	TBD	μA

Note: (1) The VPP pin is open on normal mode and in used while OTP programming condition.

Table 8.2: DC characteristic

High-speed receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID}, between the positive input pin D_p and the negative input pin D_n. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Differential input high threshold	V _{IDTH}	-	-	70	mV
Differential input low threshold	V _{IDTL}	-70	-	-	mV
Single-ended input low voltage ⁽¹⁾	V _{ILHS}	-40	-	-	mV
Single-ended input high voltage ⁽¹⁾	V _{IHHS}	-	-	460	mV
Common-mode voltage HS receive mode ⁽¹⁾	V _{CMRXDC}	70	-	330	mV
Differential input impedance	Z _{ID}	80	100	125	Ω

Note: (1) +/-70mV only for reference, related to power and ground noise on system environment, this spec need to check on panel performance to fine tune.

(2) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(3) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.7: HS receiver DC specifications

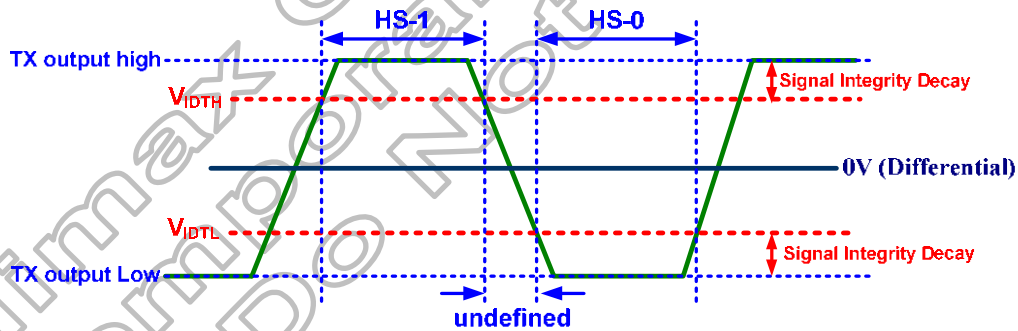


Figure 8.5: Differential HS signals for HS receive

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Common mode interference beyond 450 MHz ⁽¹⁾	$\Delta V_{CMRX(HF)}$	-	-	100	mV _{PP}
Common mode termination ⁽²⁾	C _{CM}	-	-	60	pF

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.8: HS receiver AC specifications

Low Power Mode

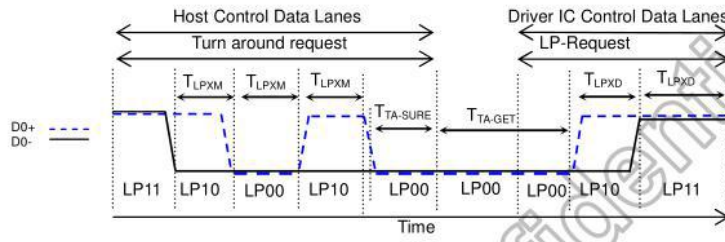


Figure 7.6: BTA from HOST to Display Module Timing

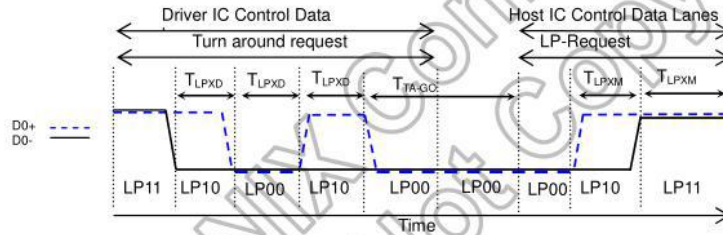


Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host → Display module	T _{LPM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module → Host	T _{LPM}	50	-	-	ns
	Time-out before the MPU start driver	T _{TA-SURE}	T _{LPM}	-	2xT _{LPM}	ns
	Time to drive LP-00 by display module	T _{TA-GET}	5xT _{LPM}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T _{TA-GET}	4xT _{LPM}	-	-	ns

Table 7.4: DSI Low Power Mode Characteristics

Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eS_{PIKE} . The filter shall allow pulses wider than T_{MIN} to propagate through the LP receiver. The related diagram shows as Figure 8.5 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

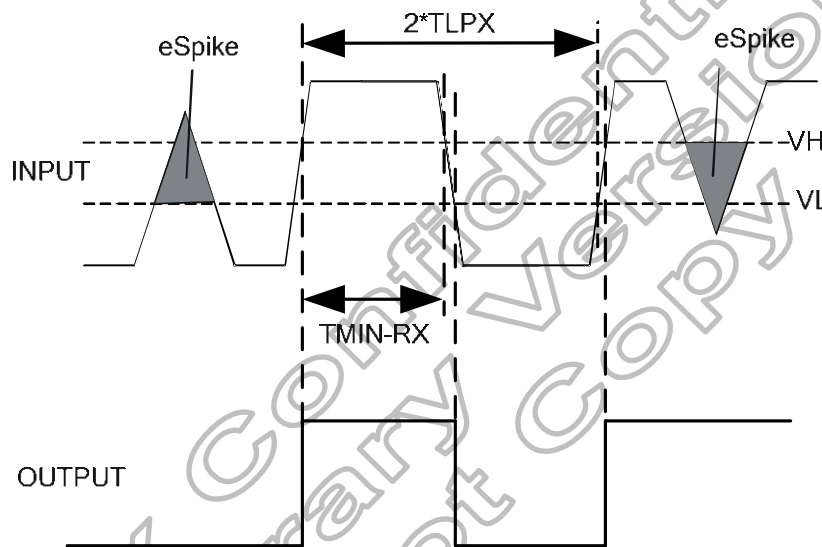


Figure 8.6: Input glitch rejections of low-power receivers

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 0 input threshold	V_{IL}	-	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	-	mV

Table 8.9: LP receiver DC specifications

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Input pulse rejection ^{(1),(2) (3)}	eS_{PIKE}	-	-	300	V.ps
Minimum pulse width response ⁽⁴⁾	T_{MIN}	20	-	-	ns
Peak-to-peak interference voltage	V_{INT}	-	-	200	mV
Interference frequency	f_{INT}	450	-	-	MHz

Note: (1) Time voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 8.10: LP receiver AC specifications

Line Contention Detection

Contention can be inferred from any of the following conditions:

- A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than V_{IL} .
- B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than V_{IH} .

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV

Table 8.11: Contention detector DC specifications

Reset input timing

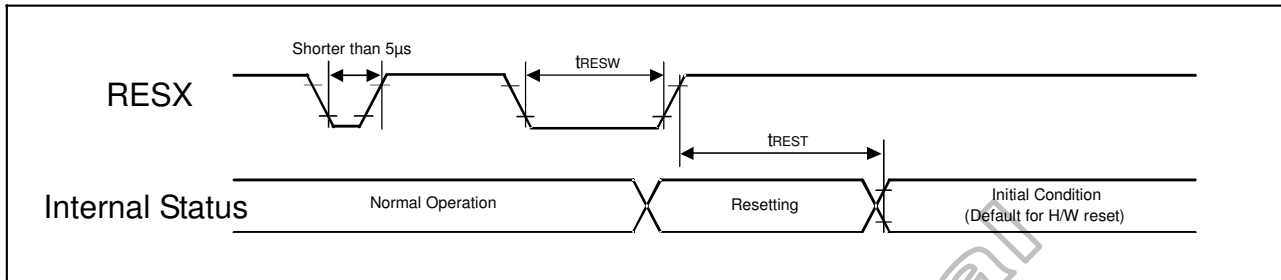


Figure 8.12: Reset input timing

Symbol	Parameter	Related pins	Spec.			Unit	Note
			Min.	Typ.	Max.		
t_{RESW}	Reset low pulse width ⁽¹⁾	RESX	10	-	-	μs	-
t_{REST}	Reset complete time ⁽²⁾	-	-	-	50	ms	-

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During Reset Complete Time, OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (**tREST**) within 5ms after a rising edge of RESX.

(3) Spike Rejection also applies during a valid reset pulse as shown below:

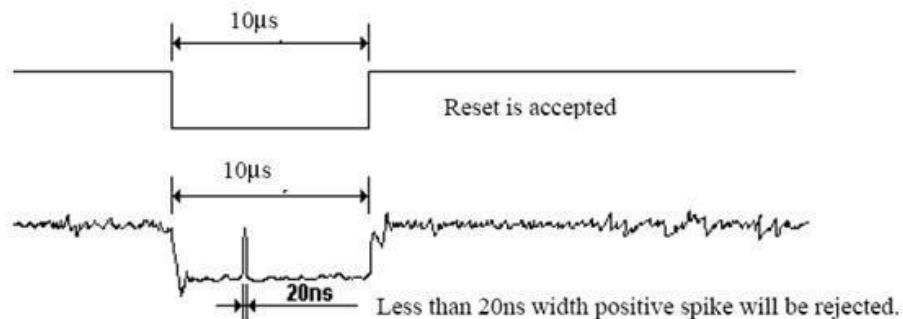


Table 8.16: Reset timing

9. Standard Specification for Reliability

9.1 Standard Specification for Reliability of LCD Module

No.	Item	Description
01	High temperature operation	The sample should be allowed to stand at 70℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 80℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -40℃ for 30 minutes → normal temperature for 5 minutes → +90℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ASTM-D-5327.
09	Electrical Static Discharge	Air: ±4KV 150pF/330Ω 5 times
		Contact: ±2KV 150pF/330Ω 5 time

*Sample size for each test item is 3~5pcs

9.2 Testing Conditions and Inspection Criteria

For the final test, the testing sample must be stored at room temperature for 24 hours. After the tests listed in Table 9.2, standard specifications for reliability will be executed in order to ensure stability.

No.	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

10. Specification of Quality Assurance

This standard of Quality Assurance confirms to the quality of LCD module products supplied by .

10.1 Quality Test

Before delivering, the supplier should conduct the following tests to confirm the quality of products.

Electrical-Optical Characteristics: According to the individual specification to test the product.

Appearance Characteristics: According to the individual specification to test the product.

Reliability Characteristics: According to the definition of reliability on the specification for testing products.

10.2 Delivery Test

Before delivering, the supplier should conduct the delivery test.

- Test method: According to MIL-STD105E.General Inspection Level II take a single Time.

The defects classify of AQL as following:

Major defect: AQL = 0.65

Minor defect: AQL = 2.5

Total defects: AQL = 2.5

10.3 Non-conforming Analysis & Deal With Manners

10.3.1 Non-conforming Analysis

Purchaser should provide the data detail of non-conforming sample and the non-conforming.

After receiving the data detail from purchaser, the analysis of non-conforming should be finished within two weeks.

- If the analysis can't be finished on time, supplier must notice purchaser 3 days in advance.

10.3.2 Disposition of non-conforming

If any product defect be found during assembling, supplier must change the good for every defect after confirmation.

Both supplier and customer should analyze the reason and discuss the disposition of non-conforming when the reason of nonconforming is not sure.

10.4 Agreement items

Both parties should negotiate together when the following problems happen.
There is any problem of standard of quality assurance, and both sides should agree that it must be modified.

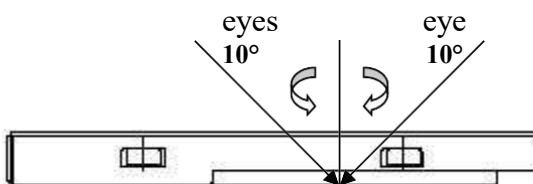
There is any argument item which does not record in the standard of quality assurance.

Any other special problem.

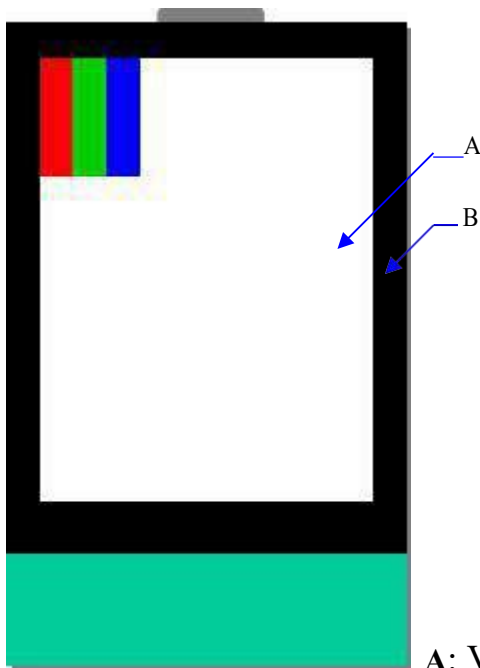
10.5 Standard of The Product Appearance Test

10.5.1 Manner of appearance test

- The test must be under $20W \times 2$ or $40W$ fluorescent light, and the distance of view must be at $30 \pm 5cm$.
When test the model of transmissive product must add the reflective plate.
- The test direction is base on around 10° of vertical line.
- Temperature: $25 \pm 5^\circ C$ Humidity: $60 \pm 10\%RH$



Definition of area:



A: Viewing area B: Outside viewing area

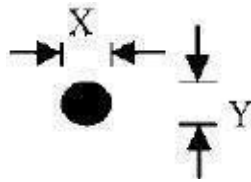
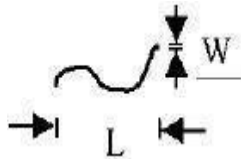
10.5.2 Basic principle

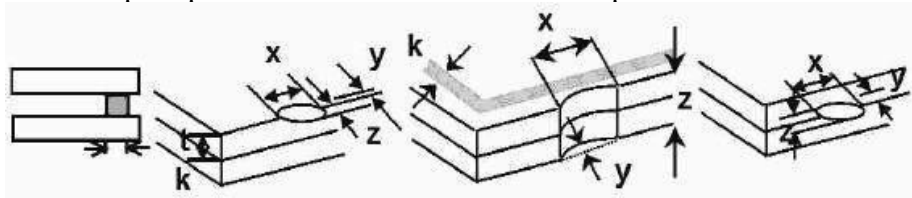
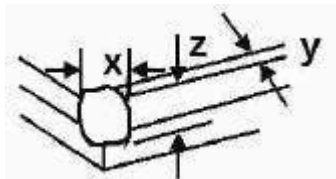
When the standard can not be described, AQL will be applied.

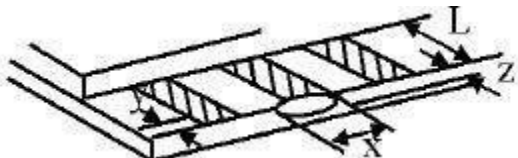
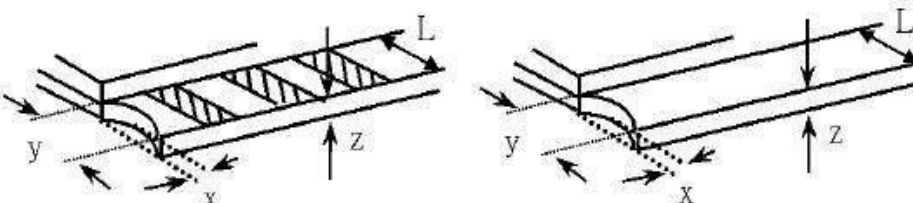
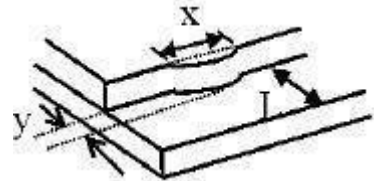
The sample of the lowest acceptable quality level must be negotiated by both supplier and customer when any dispute happened.

New item must be added on time when it is necessary.

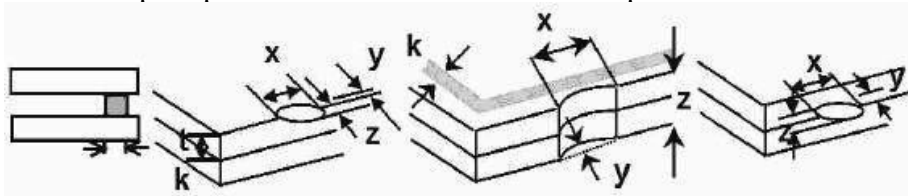
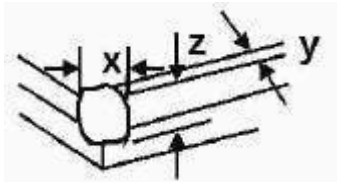
10.6 Inspection Specification

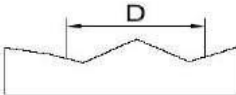
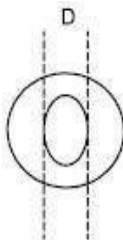
NO.	Item	Criterion	AQL																										
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 LCD viewing angle defect. 1.7 Mixed product types. 1.8 Flicker	0.65																										
02	Black or White spots or Bright spots or Color spots on LCD (Display only)	2.1 White and black or color spots on display ≦ 0.25mm, no more than Five spots. 2.2 Densely spaced: No more than three spots within 3mm.	2.5																										
03	LCD and Touch Panel black spots, white spots, contamination (non – display)	3.1 Round type: As following drawing $\Phi = (X+Y) / 2$ <table><tr><th>Size(mm)</th><th>Acceptable Q'ty</th></tr><tr><td>$\Phi \leq 0.10$</td><td>Accept no dense</td></tr><tr><td>$0.10 < \Phi \leq 0.20$</td><td>2</td></tr><tr><td>$0.20 < \Phi \leq 0.25$</td><td>2</td></tr><tr><td>$0.25 < \Phi \leq 0.30$</td><td>1</td></tr><tr><td>$0.30 < \Phi$</td><td>0</td></tr></table> * Densely spaced: No more than two spots within 3mm. 3.2 Line type: (As following drawing) <table><tr><th>Length(mm)</th><th>Width(mm)</th><th>Acceptable Q'ty</th></tr><tr><td>---</td><td>$W \leq 0.02$</td><td>Accept no dense</td></tr><tr><td>$L \leq 3.0$</td><td>$0.02 < W \leq 0.05$</td><td rowspan="2">2</td></tr><tr><td>$L \leq 2.5$</td><td>$0.03 < W \leq 0.08$</td></tr><tr><td>---</td><td>$0.08 < W$</td><td>Rejection</td></tr></table> * Densely spaced: No more than two lines within 3mm.	Size(mm)	Acceptable Q'ty	$\Phi \leq 0.10$	Accept no dense	$0.10 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	2	$0.25 < \Phi \leq 0.30$	1	$0.30 < \Phi$	0	Length(mm)	Width(mm)	Acceptable Q'ty	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.05$	2	$L \leq 2.5$	$0.03 < W \leq 0.08$	---	$0.08 < W$	Rejection	2.5
Size(mm)	Acceptable Q'ty																												
$\Phi \leq 0.10$	Accept no dense																												
$0.10 < \Phi \leq 0.20$	2																												
$0.20 < \Phi \leq 0.25$	2																												
$0.25 < \Phi \leq 0.30$	1																												
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Length(mm)	Width(mm)	Acceptable Q'ty																											
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$L \leq 2.5$	$0.03 < W \leq 0.08$																												
---	$0.08 < W$	Rejection																											

NO.	Item	Criterion			AQL
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction	Size Φ (mm)	Acceptable Q'ty	2.5
			$\Phi \leq 0.20$	Accept no dense	
			$0.20 < \Phi \leq 0.50$	3	
			$0.50 < \Phi \leq 1.00$	2	
			$1.00 < \Phi$	0	
			Total Q'ty	3	
05	Scratches	Follow NO.3 -2 Line Type.			
06	Chipped glass	Symbols: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 6.1 General glass chip: 6.1.1 Chip on panel surface and crack between panels:			2.5
					
		z: Chip thickness	y: Chip width	x: Chip length	
		$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	
		$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	
		⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip 6.1.2 Corner crack:			
					
		z: Chip thickness	y: Chip width	x: Chip length	
		$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	
		$1/2t < z \leq 2t$	Not exceed 1/3k	$x \leq 1/8a$	
		⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip			

NO.	Item	Criterion	AQL						
07	Glass crack	Symbols: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 7.2 Protrusion over terminal: 7.2.1 Chip on electrode pad: 	2.5						
		<table><tr><td>y: Chip width</td><td>x: Chip length</td><td>z: Chip thickness</td></tr><tr><td>$y \leq 0.5\text{mm}$</td><td>$x \leq 1/8a$</td><td>$0 < z \leq t$</td></tr></table>		y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$
		y: Chip width		x: Chip length	z: Chip thickness				
		$y \leq 0.5\text{mm}$		$x \leq 1/8a$	$0 < z \leq t$				
		7.2.2 Non-conductive portion: 							
<table><tr><td>y: Chip width</td><td>x: Chip length</td><td>z: Chip thickness</td></tr><tr><td>$y \leq L$</td><td>$x \leq 1/8a$</td><td>$0 < z \leq t$</td></tr></table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$			
y: Chip width	x: Chip length	z: Chip thickness							
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$							
⊙ If there chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications. ⊙ If the product will be heat sealed by the customer, the alignment mark must not be damaged. 7.2.3 Substrate protuberance and internal crack 									
		<table><tr><td>y: width</td><td>x: length</td></tr><tr><td>$y \leq 1/3L$</td><td>$X \leq a$</td></tr></table>	y: width	x: length	$y \leq 1/3L$	$X \leq a$			
y: width	x: length								
$y \leq 1/3L$	$X \leq a$								

NO.	Item	Criterion	AQL
08	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
09	Backlight elements	9.1 Illumination source flickers when lit. 9.2 Spots or scratches that appear when lit must be judged. Using LCD spot, lines and contamination standards. 9.3 Backlight doesn't light or color is wrong.	2.5 2.5 0.65
10	Bezel	Bezel must comply with product specifications.	2.5
11	PCB、COB	11.1 COB seal may not have pinholes larger than 0.2mm or contamination. 11.2 COB seal surface may not have pinholes through to the IC. 11.3 The height of the COB should not exceed the height indicated in the assembly diagram. 11.4 There may not be more than 2mm of sealant outside the seal area on PCB. And there should be no more than three places. 11.5 Parts on PCB must be the same as on the production characteristic chart, There should be no wrong parts, missing parts or excess parts. 11.6 The jumper on the PCB should conform to the product characteristic chart.	2.5 2.5 2.5 2.5 0.65 0.65
12	FPC	12.1 FPC terminal damage $\leq$ 1/2 FPC terminal width and can not affect the function , we judge accept. 12.2 FPC alignment hole damage $\leq$ 1/2 alignment area and can not affect the function , we judge accept.	2.5 2.5
13	Soldering	13.1 No cold solder joints, missing solder connections, oxidation or icicle. 13.2 No short circuits in components on PCB or FPC.	2.5 0.65

NO.	Item	Criterion	AQL												
14	Touch Panel Chipped glass	Symbols: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Touch Panel Total thickness a: LCD side length L: Electrode pad length 14.1 General glass chip: 14.1.1 Chip on panel surface and crack between panels:  <table> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td>$Z \leq t$</td> <td>$\leq 1/2 k$ and not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> </table> ⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip 14.1.2 Corner crack:  <table> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td>$z \leq t$</td> <td>$\leq 1/2 k$ and not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> </table> ⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length													
$Z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$													
z: Chip thickness	y: Chip width	x: Chip length													
$z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$													

NO.	Item	Criterion	AQL										
15	Touch Panel(Fish eye、dent and bubble on film)	<table> <tr> <th>SIZE(mm)</th> <th>Acceptable Q'ty</th> </tr> <tr> <td>$\Phi \leq 0.2$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.2 < D \leq 0.4$</td> <td>5</td> </tr> <tr> <td>$0.4 < D \leq 0.5$</td> <td>2</td> </tr> <tr> <td>$0.5 < D$</td> <td>0</td> </tr> </table>  	SIZE(mm)	Acceptable Q'ty	$\Phi \leq 0.2$	Accept no dense	$0.2 < D \leq 0.4$	5	$0.4 < D \leq 0.5$	2	$0.5 < D$	0	2.5
SIZE(mm)	Acceptable Q'ty												
$\Phi \leq 0.2$	Accept no dense												
$0.2 < D \leq 0.4$	5												
$0.4 < D \leq 0.5$	2												
$0.5 < D$	0												
16	Touch Panel Newton ring	Newton ring dimension $\leq 1/2$ touch panel area and not affect font and line distortion($\leq 2.5\%$) , it is acceptable.	2.5										
17	Touch Panel Linearity	Less than 2.5% is acceptable.	2.5										
18	LCD Ripple	Touch the touch panel , can not see the LCD ripple. Pen: R 1.0mm silicon rubber. Operation Force: 80g	2.5										
19	General appearance	19.1 Pin type must match type in specification sheet. 19.2 LCD pin loose or missing pins. 19.3 Product packaging must the same as specified on packaging specification sheet. 19.4 Product dimension and structure must conform to product specification sheet.	0.65 0.65 0.65 0.65										

11. General Precautions

11.1. Safety

- Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

11.2. Handling

- The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
- To avoid contamination on the display surface, do not touch the module surface with bare hands.
- Keep a space so that the LCD panels do not touch other components.
- Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
- Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
- Do not leave module in direct sunlight to avoid malfunction of the ICs.

11.3. Static Electricity

- Be sure to ground module before turning on power or operating module.
- Do not apply voltage which exceeds the absolute maximum rating value.

11.4. Storage

- Store the module in a dark room where must keep at $25\pm 10^{\circ}\text{C}$ and 65%RH or less.
- Do not store the module in surroundings containing organic solvent or corrosive gas.
- Store the module in an anti-electrostatic container or bag.

11.5. Cleaning

- Do not wipe the polarizer with dry cloth. It might cause scratch.
- Only use a soft cloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

12. Packing Method

----TBD