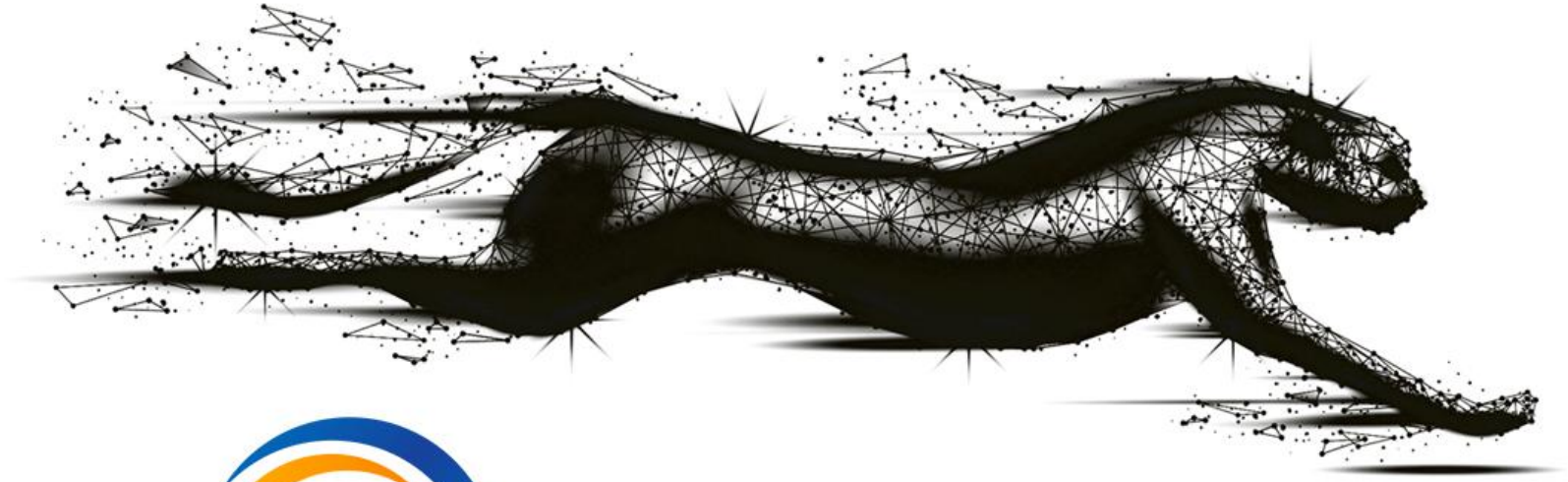
VD-RGB800480 5寸电容触摸屏

LCD模组介绍



SZOVS

深圳奥唯思，为FPGA而生...

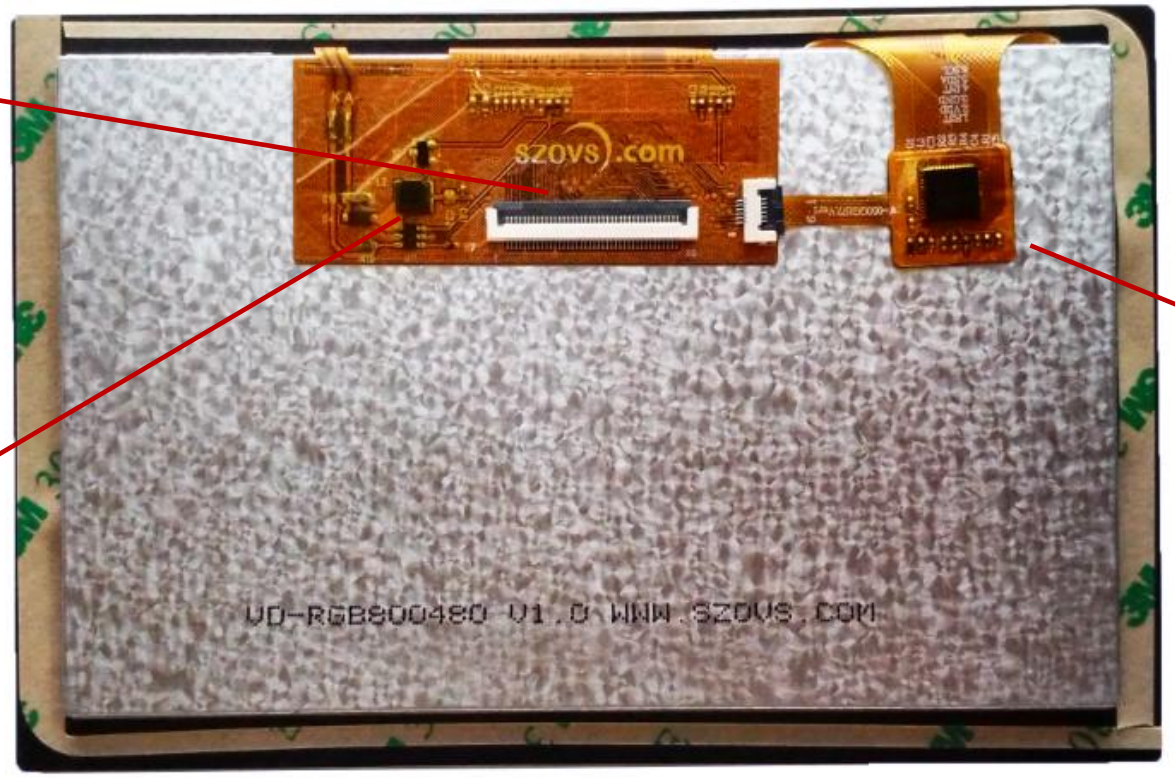
VD-RGB800480触摸屏

型号	VD-RGB800480
类型	IPS 电容屏
品牌	奥唯思
尺寸	120*75.8mm
分辨率	800*480@60Hz
接口	RGB888/RGB666/RGB565时序
触摸	汇顶科技GT911触摸芯片，支持多点触摸
接口	40P FPC接口，集成触摸IIC

VD-RGB800480触摸屏 接口介绍

40P 0.5mm下接翻盖
LCD RGB888 FPC

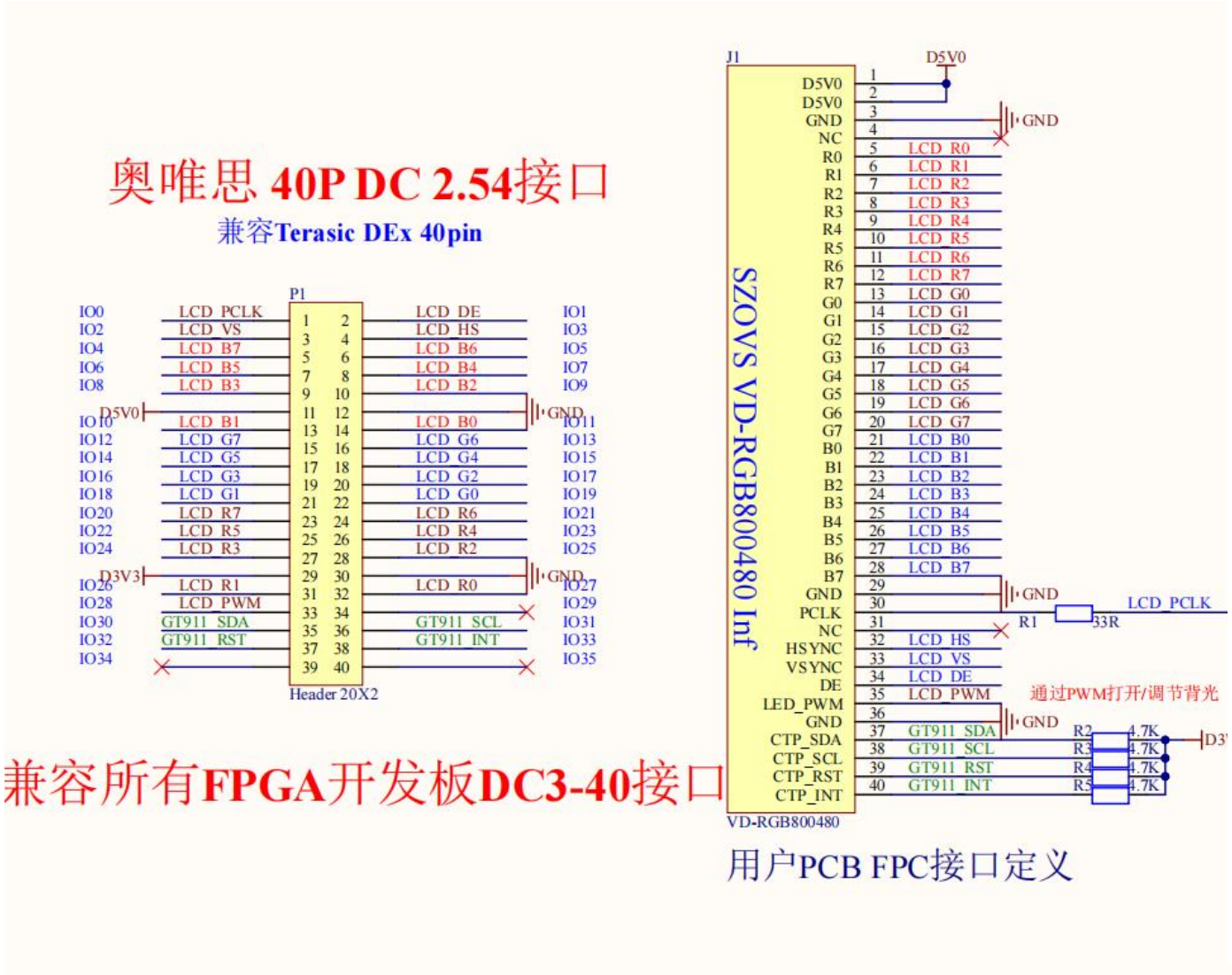
模组集成
LED背光电路



汇顶GT911
触摸芯片

全定制开模，集成背光电路，重定义LCD

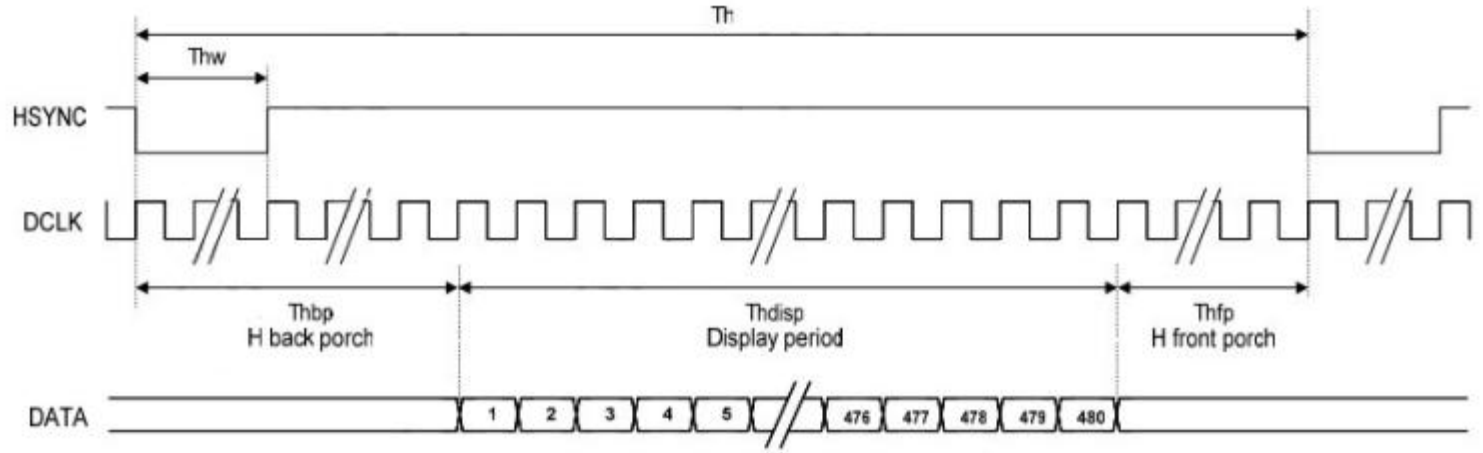
VD-RGB800480 FPC定义介绍



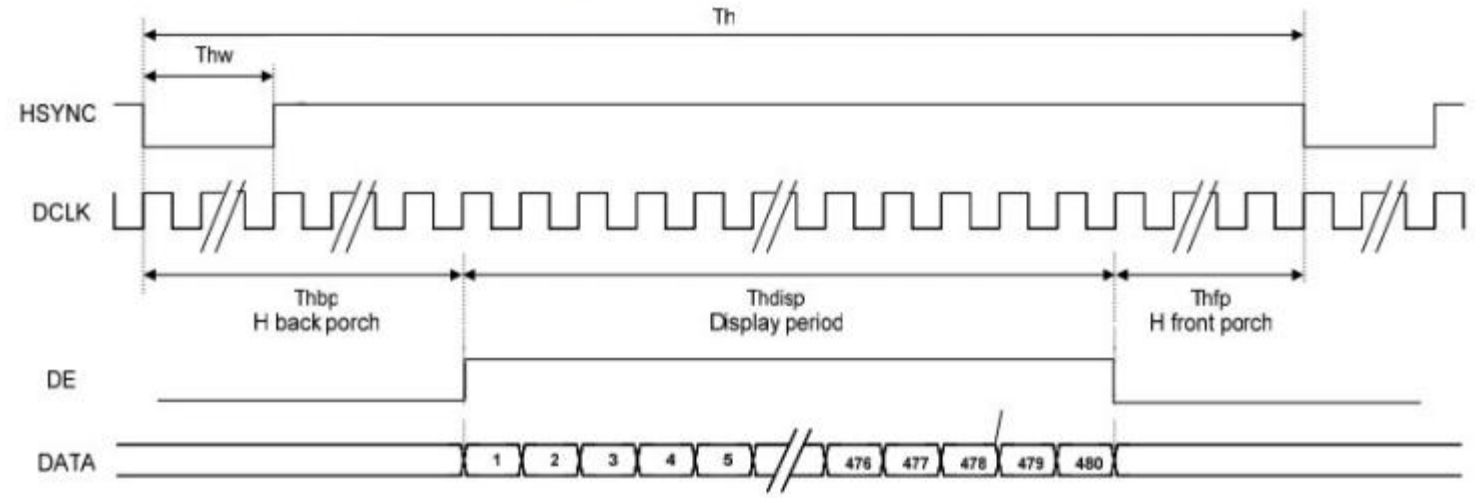
PIN NO.	SYMBOL	DESCRIPTION	REMARK
1	CTP_INT	Interrupt signal from TP	
2	CTP_RST	Reset pin for TP	
3	CTP_SCL	I2C SCL for TP	
4	CTP_SDA	I2C SDA for TP	
5	GND	Ground	
6	LED_PWM	PWM signal for LCD backlight	
7	DE	Input data enable control. When DE mode, active High to enable data input (Normally pull low)	
8	VS	Vertical sync input	
9	HS	Horizontal sync input	
10	LED_EN	enable signal for LCD backlight	
11	DCLK	Clock for input data. Data latched at rising/falling edge of this signal. Default is falling edge.	
12	GND	Ground	
13	B7	Blue data input B7.	
14	B6	Blue data input B6.	
15	B5	Blue data input B5.	
16	B4	Blue data input B4.	
17	B3	Blue data input B3.	
18	B2	Blue data input B2.	
19	B1	Blue data input B1.	
20	B0	Blue data input B0.	
21	G7	Green data input G7.	
22	G6	Green data input G6.	
23	G5	Green data input G5.	
24	G4	Green data input G4.	
25	G3	Green data input G3.	
26	G2	Green data input G2.	
27	G1	Green data input G1.	
28	G0	Green data input G0.	
29	R7	Red data input R7.	
30	R6	Red data input R6.	
31	R5	Red data input R5.	
32	R4	Red data input R4.	
33	R3	Red data input R3.	
34	R2	Red data input R2.	
35	R1	Red data input R1.	
36	R0	Red data input R0.	
37	VDD_3V3	Power supply for LCD and TP. (3.3V typ)	
38	GND	Ground	
39	VLED_5V	Power supply for LED.(5V typ)	
40	VLED_5V	Power supply for LED.(5V typ)	

VD-RGB800480 驱动时序介绍

8.3. SYNC Mode Timing Diagram



8.4. SYNC-DE Mode Timing Diagram



VD-RGB800480 行场参数描述

8.2. Timing Characteristic

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	
DCLK Frequency		Fdk	-	51	67	MHz	
DCLK Period		Tclk	-	-	-	Ns	
Hsync	Period Time	Th	-	1056	-	DCLK	
	Display Period	Thdisp		800	-	DCLK	
	To 1st Data input	Thbp	-	46	-	DCLK	By H BLANKING setting
	Front Porch	Thfp	-	210	-	DCLK	
	Pulse Width	Thw	-	4	-	DCLK	
Vsync	Period Time	Tv	-	525	-	H	
	Display Period	Tvdisp	-	480	-	H	
	Delay to 1st Gate output	Tvbp	-	23	-	H	By V BLANKING setting
	Front Porch	Tvfp	-	22	-	H	
	Pulse Width	Tvw	-	5	-	H	

```
80  //---------------------------------
81  //  800 * 480
82  `ifdef  VGA_800_480_60FPS_50MHz
83  `define H_FRONT 11'd210
84  `define H_SYNC  11'd4
85  `define H_BACK  11'd46
86  `define H_DISP  11'd800
87  `define H_TOTAL 11'd1056
88
89  `define V_FRONT 11'd22
90  `define V_SYNC  11'd5
91  `define V_BACK  11'd23
92  `define V_DISP  11'd480
93  `define V_TOTAL 11'd525
94  `endif
```

HDMI + DDR3 测试功能演示

采用FPC转接板，支持奥唯思电路所有FPGA开发板（紫光/Xilinx/Altera等）

VD-RGB800480触摸屏尺寸